Claims

[c1] 1.A digital frequency divider apparatus, comprising:
a plurality of next-state generator elements receiving an input clock signal thereto, and configured to generate a next value for each of a corresponding plurality of internal state variables;
a plurality of flip-flop elements configured to store said generated next values for said plurality of internal state variables; and
said plurality of flip-flop elements further configured to provide a present value of said plurality of internal state variables to said next-state generator elements through a feedback path therebetween;
wherein said generated next values for said plurality of internal state variables are based upon said present values of said plurality of internal state variables and said input clock signal.

[c2] 2.The apparatus of claim 1, further comprising a reset element associated with each of said next-state generator elements, said reset element configured for setting said internal state variables and their complements to a desired initial value.

[c3] 3.The apparatus of claim 1, wherein said flip-flop elements further comprise double edge triggered, D flip-flop elements.

[c4] 4.The apparatus of claim 3, wherein said double edge triggered, D flip-flop elements further comprise a pair of D flip-flops connected in parallel.

[c5] 5.The apparatus of claim 1, wherein said next-state generator elements are implemented with CMOS logic.

[c6] 6.A digital frequency divided by N divider apparatus, comprising:
plurality of next-state generator elements receiving an input clock signal thereto, and configured to generate a next value for each of a corresponding plurality of internal state variables;
a plurality of flip-flop elements configured to store said generated next values for said plurality of internal state variables;
said plurality of flip-flop elements further configured to provide a present value of said plurality of internal state variables to said next-state generator elements through a feedback path therebetween;
said generated next values for said plurality of internal state variables based upon said present values of said

plurality of internal state variables and said input clock signal; and

one or more of said next-state generator elements further configured to generate a preactivated internal state variable prior to a transition from state X to state X+1, wherein during said transition at least one of said internal state variable changes, and wherein at least one of said next value also changes as a result thereof.

[c7] 7.The apparatus of claim 6, wherein said one or more of said next-state generator elements configured to generate a preactivated internal state variable further comprises:

logic configured to detect state X;

a latch mechanism coupled to an output of said logic, said latch mechanism configured to precharge a transistor device such that a preactivated internal state variable is realized immediately upon a change in said input clock signal at state X+1.

[c8] 8.The apparatus of claim 7, further comprising a reset element associated with each of said next-state generator elements, said reset element configured for setting said internal state variables and their complements to a desired initial value.

[c9] 9.The apparatus of claim 7, wherein said flip-flop ele-

ments further comprise double edge triggered, D flip-flop elements.

[c10] 10.The apparatus of claim 9, wherein said double edge triggered, D flip-flop elements further comprise a pair of D flip-flops connected in parallel.

[c11] 11.The apparatus of claim 7, wherein said next-state generator elements are implemented with CMOS logic.

[c12] 12.A method for dividing the frequency of an input clock signal, the method comprising:
configuring a plurality of next-state generator elements to generate a next value for each of a corresponding plurality of internal state variables;
configuring a plurality of flip-flop elements for storing said generated next values for said plurality of internal state variables; and
said plurality of flip-flop elements further configured to provide a present value of said plurality of internal state variables to said next-state generator elements through a feedback path therebetween;
wherein said generated next values for said plurality of internal state variables are based upon said present values of said plurality of internal state variables and the input clock signal.

[c13] 13.The method of claim 12, further comprising configuring a reset element associated with each of said next-state generator elements, said reset element configured for setting said internal state variables and their complements to a desired initial value.

[c14] 14.The method of claim 12, wherein said flip-flop elements further comprise double edge triggered, D flip-flop elements.

[c15] 15.The method of claim 14, wherein said double edge triggered, D flip-flop elements further comprise a pair of D flip-flops connected in parallel.

[c16] 16.The method of claim 12, wherein said next-state generator elements are implemented with CMOS logic.

[c17] 17.The method of claim 12, further comprising:
determining a transition from state X to state X+1, wherein during said transition at least one of said internal state variable changes, and wherein at least one of said next value also changes as a result thereof; and
using one or more of said next-state generator elements to generate a preactivated internal state variable prior to state X+1.

[c18] 18.The method of claim 17, further comprising:
detecting state X; and

precharging a transistor device such that a preactivated internal state variable is realized immediately upon a change in said input clock signal at state X+1.